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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,462	02/20/2004	Ronald Gene Filippi	YOR920040056US1 (163-31)	7450
24336	7590	11/03/2005	EXAMINER	
KEUSEY, TUTUNJIAN & BITETTO, P.C. 14 VANDERVENTER AVENUE, SUITE 128 PORT WASHINGTON, NY 11050			FULK, STEVEN J	
			ART UNIT	PAPER NUMBER
			2891	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/783,462

Applicant(s)

FILIPPI ET AL.

Examiner

Steven J. Fulk

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 13 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) 17-31 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2/20/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: Non-patent literature.

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election with traverse of Group I, claims 1-16, in the reply filed on 13 October 2005 is acknowledged. The traversal is on the ground(s) that the features and aspects of the claims are such that serious burden would not be placed on the Examiner to search the comment subject. This is not found persuasive because the accepted tests set forth in MPEP § 803 for establishing a prima facie case of burden have been satisfied, as such the burden has shifted to the applicant and the applicant has failed to rebut.

The requirement is still deemed proper and is therefore made FINAL.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. (NPL Reference "U") in view of Huston et al. (NPL Reference "V").

Ogawa et al. discloses a method for evaluating reliability of a semiconductor chip structure built by a manufacturing process, comprising the steps of: building a dual damascene test structure with vias having conductive liners along the bottoms and sidewalls of the vias (p. 313, col. 1), which uses materials having mismatches in coefficients of thermal expansion (copper and oxide) providing a uniform stress

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on the structure (p. 316, col. 2; Fig. 8), the test structure including features having predetermined strain values; thermal cycling electrically functional test structures to induce changes or failures of the features (p. 313, col. 2; Fig. 2); measuring the yield of the features in the test structure (resistance shift/device failure) (p. 312, col. 2).

Ogawa et al. does not teach evaluating reliability of the semiconductor chip structure built by the manufacturing process based on the yield. Huston et al. teaches a method of evaluating the reliability of a semiconductor chip using a test structure built by the same manufacturing process (p. 271, col. 1), wherein the evaluation results in early and late fails and the reliability is based on early fails (p. 268, col. 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the reliability evaluation method of Huston et al. in the test method of Ogawa et al. because relating test structure yield to product reliability is a conventional practice in semiconductor manufacturing to improve product performance and reduce production costs.

### ***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. Langer et al. '786 and Werner et al. '901 disclose methods of evaluating thermal stress failure in the damascene process of a semiconductor device.

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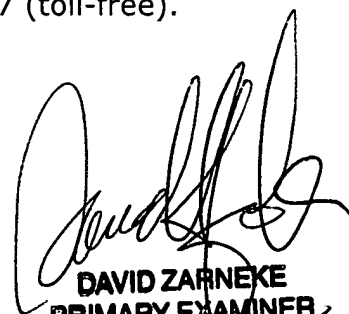
b. Ryan '587, Akram et al. '750, and Fasano et al. '669 disclose methods of evaluating thermal stress failure in a metal line of a semiconductor device.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf  
10/26/05

  
**DAVID ZARNEKE**  
**PRIMARY EXAMINER**  
10/28/05